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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,678	07/02/2003	William Mar	3304.2.65	3447

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,678	MAR ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on August 02, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the Examiner.

Oath/Declaration

The Oath filed July 02, 2003 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings filed July 02, 2003 are accepted.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

> ***The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often***

used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title or claim(s). It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it exceeds 150 words.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

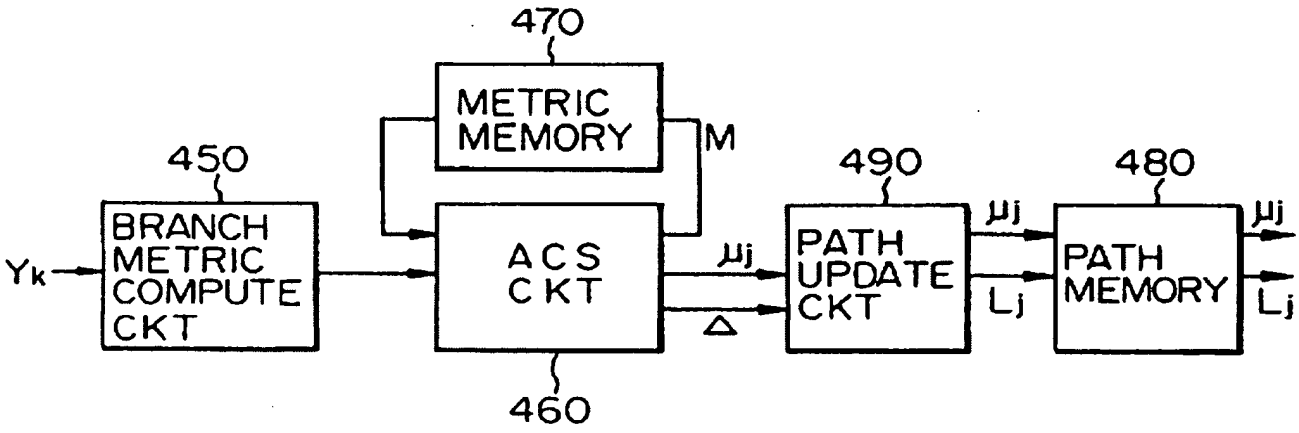
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuragawa et al. (USPN 5907586) further in view of Itakura et al. (USPN 5418795).

As per claim 1, Katsuragawa et al. (herein after referred to as one entity: Katsuragawa) substantially teaches (abstract) a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of

probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Particularly, Katsuragawa teaches (Figure 7) a branch metric unit 450, a add-compare-select unit 460, a metric memory 470, a decision unit 490 and a survivor memory 480.

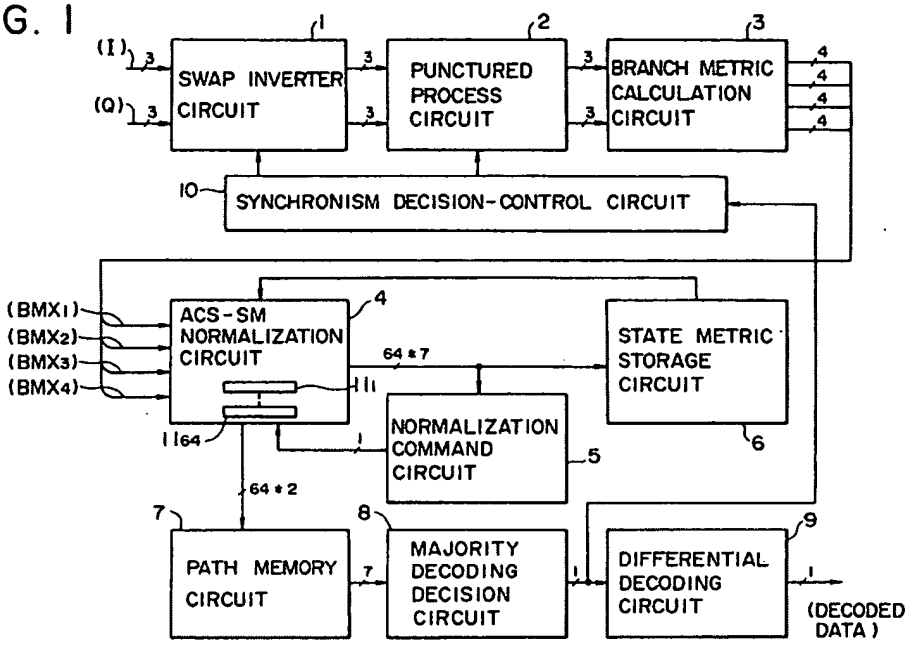
Fig. 7



Katsuragawa does not explicitly teach a multi-data input as stated in the present application.

However, Itakura et al. (herein after referred to as one entity: Itakura), in an analogous art, teaches a Viterbi decoding apparatus includes a brand metric calculation circuit for calculating a branch metric for a plurality of time slots at one time by an add-compare-select-state-metric (ACS-SM) calculation circuit for performing add-compare-select (ACS) calculation an add-compare-select-state-metric calculation circuit according to a branch metric for a plurality of time slots obtained by the branch metric calculation circuit and a state metric in the preceding stage at intervals of a plurality of time slots, and a maximum likelihood sequence decision circuit for decoding input data according to the content of the path obtained through the ACS calculation, wherein on the outside of a loop composed of the ACS-SM normalization circuit and a state metric storage circuit, there is provided a normalization command circuit, whereby a decision as to the necessity for normalization, a setting of the timing of normalization, and the like are performed, and, when it is decided that normalization is necessary, the state metric normalized through a bit shifting process in the ACS-SM normalization circuit is selected before at least any one of the state metrics overflows and the selected state metric is output as a new state metric.

FIG. 1

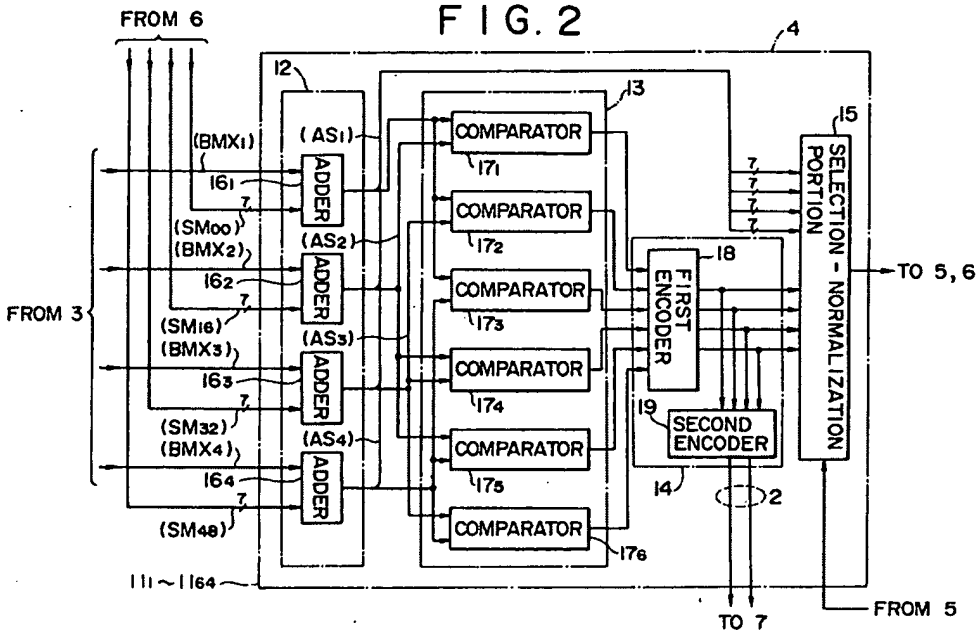


Itakura teaches (Figure 1) a multi-data input for the decoding device. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to modify the teachings of Katsuragawa by having a multi-data input for the decoding device. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by having a multi-data input for the decoding device would have increased decoding speed.

As per claim 2, Katsuragawa substantially teaches, in view of above rejection, (Figure 7 and cols. 15-16) the difference delta an index showing what kinds of paths are compared and selected at each of the consecutive branches. The difference or index and the path selected are fed to the path update circuit 490 while the path metric of the path selected is written to the metric memory 470.

As per claims 3 and 8, Itakura substantially teaches, in view of above rejection, (Figure 2) a plurality of accumulators, comparators and selectors.

FIG. 2



As per claims 4 and 5, Katsuragawa substantially teaches, in view of above rejection, (Figure 1) a plurality of path memories.

As per claim 6, Katsuragawa et al. (herein after referred to as one entity: Katsuragawa) substantially teaches (abstract) a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS

circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Particularly, Katsuragawa teaches (Figure 7) a branch metric unit 450, a add-compare-select unit 460, a metric memory 470, a decision unit 490 and a survivor memory 480.

Katsuragawa does not explicitly teach a multi-data input as stated in the present application.

However, Itakura et al. (herein after referred to as one entity: Itakura), in an analogous art, teaches a Viterbi decoding apparatus includes a brand metric calculation circuit for calculating a branch metric for a plurality of time slots at one time by an add-compare-select-state-metric (ACS-SM) calculation circuit for performing add-compare-select (ACS) calculation an add-compare-select-state-metric calculation circuit according to a branch metric for a plurality of time slots obtained by the branch metric calculation circuit and a state metric in the preceding stage at intervals of a plurality of time slots, and a maximum likelihood sequence decision circuit for decoding input data according to the content of the path obtained through the ACS calculation, wherein on the outside of a loop composed of the ACS-SM normalization circuit and a state metric storage circuit, there is provided a normalization command circuit, whereby a decision as to the necessity for normalization, a setting of the timing of normalization, and the like are performed, and, when it is decided that normalization is necessary, the state metric normalized through a bit shifting process in the ACS-SM normalization circuit is selected before

at least any one of the state metrics overflows and the selected state metric is output as a new state metric. Itakura teaches (Figure 1) a multi-data input for the decoding device. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to modify the teachings of Katsuragawa by having a multi-data input for the decoding device. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by having a multi-data input for the decoding device would have increased decoding speed.

As per claim 7, Katsuragawa substantially teaches, in view of above rejection, (Figure 7 and cols. 15-16) the difference delta an index showing what kinds of paths are compared and selected at each of the consecutive branches. The difference or index and the path selected are fed to the path update circuit 490 while the path metric of the path selected is written to the metric memory 470.

As per claims 9-13 , Katsuragawa substantially teaches, in view of above rejection, (Figure 7) the metric memory 470 may advantageously be implemented by a plurality of latch circuits capable of sequentially updating the path metrics selected by the ACS circuit 460, and feeding back the updated path metrics to the ACS circuit 460 branch by branch, as in the previous embodiment. The path memory 480 sequentially updates the path selected by the ACS circuit 460. Particularly, in this embodiment, the path memory 480 stores the reliability information of the path together with the path.

As per claim 14, Katsuragawa et al. (herein after referred to as one entity: Katsuragawa) substantially teaches (abstract) a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A

plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Particularly, Katsuragawa teaches (Figure 7) a branch metric unit 450, a add-compare-select unit 460, a metric memory 470, a decision unit 490 and a survivor memory 480.

Katsuragawa does not explicitly teach a multi-data input as stated in the present application.

However, Itakura et al. (herein after referred to as one entity: Itakura), in an analogous art, teaches a Viterbi decoding apparatus includes a brand metric calculation circuit for calculating a branch metric for a plurality of time slots at one time by an add-compare-select-state-metric (ACS-SM) calculation circuit for performing add-compare-select (ACS) calculation an add-compare-select-state-metric calculation circuit according to a branch metric for a plurality of time slots obtained by the branch metric calculation circuit and a state metric in the preceding stage at intervals of a plurality of time slots, and a maximum likelihood sequence decision circuit for decoding input data according to the content of the path obtained through the ACS

calculation, wherein on the outside of a loop composed of the ACS-SM normalization circuit and a state metric storage circuit, there is provided a normalization command circuit, whereby a decision as to the necessity for normalization, a setting of the timing of normalization, and the like are performed, and, when it is decided that normalization is necessary, the state metric normalized through a bit shifting process in the ACS-SM normalization circuit is selected before at least any one of the state metrics overflows and the selected state metric is output as a new state metric. Itakura teaches (Figure 1) a multi-data input for the decoding device. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to modify the teachings of Katsuragawa by having a multi-data input for the decoding device. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by having a multi-data input for the decoding device would have increased decoding speed.

As per claim 15, Katsuragawa substantially teaches, in view of above rejection, (Figure 7 and cols. 15-16) the difference delta an index showing what kinds of paths are compared and selected at each of the consecutive branches. The difference or index and the path selected are fed to the path update circuit 490 while the path metric of the path selected is written to the metric memory 470.

As per claims 16-19, Katsuragawa substantially teaches, in view of above rejection, a convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of 2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to a two-bit one-symbol convolutional code

with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
October 19, 2005

GUY LAMARRE
PRIMARY EXAMINER